REMARKS

This is in response to the Office Action of 12 March 2004. Claims 1-10, are pending in the application, and Claims 1-10 have been rejected.

By this Response, various non-narrowing amendments have been made to the Claims, arguments traversing the rejections of Claims 1-10 are presented, and new Claims 11-18 have been added.

No new matter has been added.

In view of the remarks below, Applicants respectfully request reconsideration and further examination.

About The Invention

The present invention relates generally to methods and apparatus for controlling a voltage multiplier. More particularly, the invention relates to methods and apparatus for directly connecting a supply voltage to the output of a voltage multiplier during a start period so as to provide a stable voltage at that output.

Non-narrowing Amendments to Claims 1-10

Various grammatical and formatting amendments have been made to the Claims. For example, the reference numerals and signal names that appear in parentheses in Claims 1-10 have been deleted. Similarly, the preambles of the dependent Claims have been amended to begin with the word "The" rather than the word "A". A spelling correction and grammatical corrections have been made in Claim 7. No reduction in the scope of the Claims is intended by these amendments.

Rejections under 35 USC 102(b)

Claims 1-10 have been rejected under 35 USC 102 (b) as being anticipated by Yanagawa (US Patent 5,994,888). More particularly, the

Examin r states that Yanagawa discloses in Fig. 1, a circuit comprising a voltage multiplier (14); a start control unit having a comparator (21-24 and 26), a logic unit (12), and a subvoltage generating unit (remainder of circuit), all connected and operating similarly as recited by Applicant.

For at least the reasons set forth below, Applicant respectfully traverses the rejections under 35 USC 102(b), and request that these rejections be withdrawn.

Yanagawa discloses circuit arrangements for operating a voltage level detector for selected limited periods of time, rather than continuously, so as to eliminate the power consumption that occurs with continuous, as opposed to part-time, operation of the voltage level detector. As can be seen in Fig. 1 of Yanagawa, both the voltage divider (R1, R2), and the comparator (21-24), have transistors in series therewith (i.e., transistors 25 and 26 respectively). Series coupled transistors 25 and 26 act to provide a path to ground for the voltage divider and the comparator only during periods when the pulse generator 20 provides an appropriate signal to those transistors. In this way current is not continuously flowing through the voltage divider and the comparator.

Applicant respectfully asserts that the limitations recited in Claims 1-10 are not met by the disclosure of Yanagawa. For example, each of Applicant's Claims 1-10 recites either the structure for, or the action of, providing the supply voltage (e.g., Vdd) as the output of the voltage multiplier during a start period. This is referred to as "direct mode" in the specification and Claims, because the supply voltage is directly connected to the output of the voltage multiplier (see page 3, lines 14-18; page 3, lines 29-32; page 5, lines 1-15; page 5, lines 26-27; page 6, lines 1-5; page 9, lines 1-5; page 10, lines 10-24; and Figs. 1, 4, and 5). This direct mode of operation occurs during a "start time". Yanagawa does disclose the direct connection of the supply voltage to the output of the voltage multiplier.

Since Yanagawa does not disclose, suggest or provide motivation for the invention as defined by Applicant's Claims 1-10, the rejections under 35 USC

102(b) are improper and should be withdrawn.

New Claims 11-18

New Claims 11-15 depend directly of indirectly from independent Claim 1, and are directed to additional structural details of the present invention, including the plurality of intermediate nodes in the subvoltage generator; the switching array between the subvoltage generator and the comparator; the band gap circuit for providing the reference voltage; and a second comparator coupled to receive a subvoltage that is different from that received by the other comparator which is coupled to the subvoltage generator through the switching array. New Claims 16-18 depend directly or indirectly from independent Claim 10, and are directed to additional operations including producing the reference voltage from a band gap circuit; and selecting subvoltages to be supplied to the comparators by means of a switching device. Support for new Claims 11-18 can be found in the specification at pages 8-9 and in Figs. 1 and 4.

Conclusion

All of the rejections in the outstanding Office Action of 12 March 2004 have been responded to, and Applicant respectfully submits that the pending Claims 1-18 are now in condition for allowance.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

By Raymond J. Werner

Raymond J. Werner
Reg. No. 34,752

Dated: 14 May 2004
Portland, Oregon